

**REMARKS**

Claims 1-27 are currently pending in which claims 1-8 are allowed. In the Office Action, claims 9, 17, 19, 20 and 24-27 were rejected under 35 U.S.C. §102(b) as being anticipated by US Pat. No. 6,037,811 to Ozguc (hereinafter "Ozguc"), and claims 10 and 11 were rejected under 35 U.S.C. §103(a) as being unpatentable over Ozguc in view of US Pat. No. 6,731,151 to Doutreloigne (hereinafter "Doutreloigne").

Claims 12-16, 18, and 21-23 were objected to as being dependent upon a rejected base claim but were otherwise considered allowable.

Applicant filed a Reply (Amendment and Request for Reconsideration) on November 18, 2005 in response to the Final Office Action mailed September 20, 2005. In the following Advisory Action mailed November 30, it was stated that the Reply was not in compliance with 37 CFR 1.121 since page 16 of the Reply was missing. Applicant respectfully submits that this non-compliance was not intentional since Applicant believes that all pages of the Reply were submitted via facsimile. Applicant's records indicate that all pages were faxed successfully, but Applicant has decided not to contest the missing page at this time. Consequently, the amendments contained within the Reply were not entered.

Applicant requests that the non-entered amendments in the Reply remain non-entered and submits the present amendments instead in order to place the present Application in a condition for allowance.

Applicant's representative, Gary Stanford (Reg. No. 35, 689), conducted a telephonic interview with Examiner Tuan T. Lam on November 28, 2005. The claims discussed were the rejected independent claims 9 and 19. During the interview, Applicant argued that the proposed amendment in the non-entered Reply were sufficient to place the condition in allowance. In particular, Applicant's position is that the current sources 122 and 152 in Ozguc (FIG. 1) are in a current-mirror configuration with output transistors MP1 and MN1 to control the current through the output transistors but that separate switches 128 and 158 are employed to switch on and off the output transistors MP1 and MN1. Agreement was not reached.

During the interview, Applicant suggested in the alternative amending claims 9 and 19 to include language in the allowed claim 1, particularly including the language further describing the multilevel pulse as "having a first large current pulse with short duration followed by at least one smaller current pulse of longer duration and sufficient to turn on and off the P-channel and N-channel devices." The Examiner stated that an Advisory Action would follow and that Applicant would be provided the opportunity in response to the Advisory Action to submit the proposed amendments.

In accordance with that suggested by Applicant during the interview, claim 9 is amended to recite "a multi-level current pulse generator that provides at least one predetermined multi-level current pulse to said gates of said P-channel and N-channel devices having a first large current pulse with short duration followed by at least one smaller current pulse of longer duration and sufficient to switch on and off said P-channel and N-channel devices while minimizing average power dissipation." Also, claim 19 is amended to recite "~~generating~~ providing at least one predetermined multi-level current

pulse ~~suffieient~~ to ~~medulate~~ the gates of a P-channel device and an N-channel device having a first large current pulse with short duration followed by at least one smaller current pulse of longer duration and sufficient to turn on and off the P-channel and N-channel devices with reduced average power dissipation.”

The Advisory Action included an Interview Summary including the Examiner’s rendition of the interview. Although Applicant agrees with most of the summary, Applicant does not recall that it was stated that allowance would be “dependent upon further search” as stated in the Examiner’s summary. Applicant does not believe that this is required or necessary to properly dispose of this cases since the proposed language directly mirrors the language of allowed claim 1 so that further search is unwarranted, unnecessary and improper.

Applicant respectfully submits that claims 9 and 19 are amended to include language contained within allowed claim 1, so that these claims are allowable over Ozguc and Doutreloigne. Applicant requests withdrawal of the rejections and allowance of all of the claims.

For completeness of the record, Applicant reiterates the arguments presented in the un-entered Reply filed November 18, 2005:

Applicant respectfully traverses the §102(b) rejection of claims 9, 17, 19, 20 and 24-27 as being anticipated by Ozguc.

Preliminarily, Applicant deems it expedient to contrast the current-controlled output buffer of Ozguc with Applicant’s illustrated embodiment, which is intended as an

embodiment of the invention only and not intended to limit Applicant's invention as recited in the claims, and. With reference to FIG. 2 of Applicant's disclosure, the tri-level pulse translator 107 generates multi-level current pulses IA and IB. The current pulse IA is mirrored and amplified by current mirrors 203 and 205 to sink current from the gate of QN to turn it fully off. The current pulse IA is mirrored and amplified by current mirrors 203 and 207 to sink current from the gate of QP to turn it fully on. The current pulse IB is mirrored and amplified by current mirror 209 to source current to the gate of QN to turn it fully on. The current pulse IB is mirrored and amplified by current mirror 209 to source current to the gate of QP to turn it fully off. In this manner, current pulse IA turns QP fully on and QN fully off to cause QP to pull the PGATE node high to PVCC. And current pulse IB turns QP fully off and QN fully on to cause QN to pull the PGATE node low to PGND. In this manner, the multi-level current pulses are provided to the gates of the P and N channel devices to switch the devices from one state to another.

In FIG. 1 of Ozguc, the control circuit 110 receives a CONTROL signal and in response, controls either I1 to produce a charging current  $I_{chg}$  sourced to OUT, or I2 to produce a discharging current  $I_{dis}$  sunk from OUT. MP1 is turned on and off separately by switch 128 and MN1 is turned on and off separately by switch 158. FIG. 2 of Ozguc works in substantially the same manner. In summary, the currents I1 and I2 are NOT intended to turn on and off MP1 or MN1, respectively; instead, these currents are controlled and mirrored to control the output charging and discharging currents.

Applicant respectfully submits that Ozguc does not show a multi-level current pulse generator that provides a multi-level current pulse to gates of P-channel and N-

channel devices *sufficient to switch the devices* while minimizing average power dissipation as recited in claim 9. Contrary to that stated in the Office Action, the variable currents I1 and I2 are NOT sufficient to switch MP1 and MP2. Instead, as clearly shown and described in Ozguc, separate switches are used to turn on and off the transistors MP1 and MP2. As shown in FIG. 1 of Ozguc, separate switches 128 and 158 controlled by a separate SIGNAL are used to turn on and off the transistors MP1 and MP2. This is described by Ozguc on col. 2, lines 21-23, which states “[a]n input signal 101 controls switches 128 and 158 to alternately activate the charging and discharging transistors MP1 and MN1.” Once MP1 is activated by switch 128, “[t]he first reference current I1 is mirrored to a charging transistor MP1 to supply a charging current Ichg to the OUT terminal.” And the discharging circuit 150 operates in a similar manner (Ozguc col. 2, line 15). Once MN1 is activated by SIGNAL controlling switch 158, “[t]he second reference current I2 is mirrored to a discharging transistor MN1 to sink (remove) a discharging current Idis from the load 160 coupled to OUT terminal” (Ozguc col. 2, lines 18-20).

The same is true for the current-controlled output buffer implementation shown in FIG. 2 of Ozguc. In that case, the adjustable current sources 222 and 252 of Ozguc do NOT operate to switch the transistors MP1 and MN1. Instead, SIGNAL is provided directly to the gate of the PMOS transistor 228 to turn on and off the transistor MP1, and SIGNAL controls activation of transistor 206a, which controls activation of transistors 204b and 206b, which control activation of transistor 258, which turns on and off transistor MN1. (Note that when SIGNAL is pulled high, transistor 206a is turned on, which pulls the gate of 204b low to turn it on, which pulls the gate of transistor 258 high

to turn it on, which grounds the gate of MN1 to turn it off.) In Ozguc's configuration, the current  $I_1$  is not used to turn on or off MP1, but instead the current  $I_1$  is mirrored as current  $I_{ch}$  through the source/drain current path of MP1. As described in Ozguc, "[a] current  $I_{chg}$  in the amount of  $K \cdot I_1$  is supplied to the output terminal via charging transistor MP1, where  $K$  (e.g., 64) is the ratio between the gates sizes of MP1 and the cascode configuration of the current source 224" (Ozguc, col. 3, line 67 to col. 4, line 3). And similarly, "a current  $I_{dis}$  in the amount of  $K \cdot I_2$  is sunk from the output terminal via discharging transistor MN1, where  $K$  (e.g., 64) is the ratio between the gate sized of MN1 and the cascode configuration of the current source 254" (Ozguc, col. 3, lines 33-36).

In summary, and contrary to that stated in the Office Action, the variable currents  $I_1$  and  $I_2$  are NOT sufficient to switch the P and N channel devices MP1, MN1 on and off, but rather these currents are mirrored through the MP1 and MN1, respectively, to control the charging and discharging currents at the output.

And the Examiner misreads the adjustable current mirror configuration shown in FIG. 4 of Ozguc. The current mirror configuration is not configured to provide a multi-level current pulse to the gates of MP1 or MN1 to switch these devices while minimizing average power dissipation. As noted above, the current  $I_1$  generated at the output of the current mirror is not used to switch the transistors but instead is mirrored through the output transistors MP1, MN1. And further, the adjustable current mirror configuration does not output a multi-level current pulse but instead is statically programmed to set the GAIN between the currents  $I_1'$  and  $I_1$ . In Ozguc, it is stated that "[i]f a longer rise time and consequently, smaller  $I_{chg}$  is desired,  $I_1$  can be decreased by replacing the high signal at DNB with a low signal, thereby switching the DOWN cascode FET pair off"

(Ozguc col. 4, lines 27-30); and “[i]f a shorter rise time and accordingly a larger  $I_{chg}$ , the UP cascode pair can be activated” (Ozguc col. 4, lines 41-43). But in either case, the DNB terminal OR the UP terminal is FIXED to a statically programmed level. Ozguc clearly describes that “[t]he programming of the DNB terminal can be accomplished by a variety of methods including wire bonding to a pad connected to DNB, using metal mask options or using programmable elements (e.g., fusible links, reprogrammable memory cell, etc.)” (Ozguc, col. 4, lines 32-36), all of which are fixed programming methods.

Furthermore, the currents  $I_1$  and  $I_2$  in Ozguc are not predetermined. As described in the prior amendment, Applicant’s multi-level current pulse is predetermined and sufficient to switch the devices while minimizing average power dissipation. In contrast, the adjustable current sources 122 and 152 (or 222 and 252) in Ozguc do not provide a predetermined multi-level current pulse but are instead controlled by the CONTROL signal to control the rise and fall times of the OUT signal.

Applicant respectfully submits, therefore, that claim 9 is allowable over Ozguc. Claim 17 is allowable as depending upon an allowable base claim. Applicant requests withdrawal of this rejection.

Further with respect to claim 17, Ozguc does not show a multi-level current pulse generator which provides a first multi-level current pulse to turn off an N-channel device and which provides a second multi-level current pulse to turn off a P-channel device. Contrary to that stated in the Office Action, neither of the pulses  $I_1$  or  $I_2$  are used to turn off the N or P channel transistors. As shown in FIG. 1 of Ozguc, separate switches 128 and 158 controlled by a separate SIGNAL are used to turn off the transistors MP1 and

MP2. And in FIG. 2 of Ozguc, the transistors 228 and 258, each controlled by SIGNAL, are used to turn on or off the transistors MP1 and MN1, respectively.

Ozguc also does not show or describe a method of driving a high voltage switching device using a gate driver implemented using a low voltage process including generating at least one predetermined multi-level current pulse sufficient to modulate the gates of a P-channel device and an N-channel device with reduced average power dissipation as recited in claim 19. As described in the prior amendment, the multi-level current pulse is predetermined and sufficient to switch the devices while minimizing average power dissipation. In contrast, the adjustable current sources 122 and 152 (or 222 and 252) in Ozguc do not provide a predetermined multi-level current pulse but are instead controlled by the CONTROL signal to control the rise and fall times of the OUT signal.

Applicant respectfully submits that claim 19 is allowable over Ozguc. Claims 20 and 24-27 are allowable as depending upon an allowable base claim. Applicant requests withdrawal of this rejection.

Further with respect to claims 25 and 26, Ozguc does not show a method including applying a first multi-level current pulse to the gate of an N-channel device to turn the N-channel device off or applying a second multi-level current pulse to the gate of the P-channel to turn it off. As described above, neither of the currents I1 or I2 in Ozguc are used to turn on or off the MP1 or MN1 transistors since separate switches are employed for this purpose.



Applicant respectfully traverses the §103(a) rejection of claims 10 and 11 as being unpatentable over Ozguc in view of Doutreloigne. As noted above, claim 9 is allowable over Ozguc and claims 10 and 11 are allowable as depending upon an allowable base claim. Doutreloigne does not overcome the deficiencies of Ozguc as noted above, so that claims 10 and 11 are allowable over Ozguc in view of Doutreloigne. Applicant requests withdrawal of this rejection.

None of the amendments made herein were related to the statutory requirements of patentability, but instead were made for purposes of clarity and/or to remove extraneous and/or unnecessary language. Also, none of the amendments were made for the purpose of narrowing the scope of any claim.

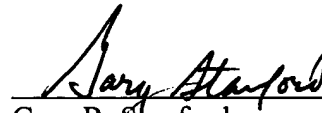
CONCLUSION

Applicant respectfully submits that for the reasons recited above and for various other reasons, the claims are allowable and the objections and rejections should be withdrawn. Reconsideration of the rejections and objections are respectfully requested. Should this response be considered inadequate or non-responsive for any reason, or should the Examiner have any questions, comments or suggestions that would expedite the prosecution of the present case to allowance, Applicants' undersigned representative earnestly requests a telephone conference.

Respectfully submitted,

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